Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUT 1**
2. **IN 1-**
3. **IN 1+**
4. **GND**
5. **IN 2+**
6. **IN 2-**
7. **OUT 2**
8. **VCC**

**.029”**

**.030”**

**7 6 5**

**1 2 3**

**8 4**

**MASK  
REF**

**393**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND or FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .029” X .030” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: LM193**

**DG 10.1.2**

#### Rev B, 7/1